AMENDMENTS TO THE CLAIMS

1. (currently amended) An array architecture for a memory device, comprising a memory cell block comprising an even number of memory cells and a transistor, wherein said memory cells are electrically coupled to said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor, said memory cells comprising variable resistance memory elements,

wherein at least two memory cells are electrically coupled to each side of said transistor.

2. canceled

3. canceled

4. (Previously Presented) The array architecture of claim 1, wherein each memory cell is in electrical communication with a respective bit line, and at least half of the bit lines are in electrical communication with a sensing circuit.

5. (currently amended) ~~The array architecture of claim 1,~~ An array architecture for a memory device, comprising a memory cell block comprising an even number of memory cells and a transistor, wherein said memory cells are electrically coupled to said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor, said memory cells comprising variable resistance memory elements,

wherein each memory cell is in electrical communication with a respective bit line and upon addressing a first memory cell of said memory cell block a sneak path

includes any second memory cell of said memory cell block that is electrically coupled to a same side of said transistor as said first memory cell and any third memory cell electrically coupled to a same bit line as said first and second memory cells.

6. canceled

7. (currently amended) ~~The array architecture of claim 1,~~ An array architecture for a memory device, comprising a memory cell block comprising an even number of memory cells and a transistor, wherein said memory cells are electrically coupled to said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor, said memory cells comprising variable resistance memory elements,

wherein each memory cell is in electrical communication with a respective bit line, a gate of said transistor is electrically coupled to a wordline and a sneak path resistance is $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$, where R is a combined resistance of each memory cell of said sneak path, n is a number of memory cells of said memory cell block electrically coupled to a same side of said transistor as an addressed memory cell, and m is a total number of wordlines of the array architecture.

8-12. canceled

13. (original) The array architecture of claim 1, wherein said memory cells comprise PCRAM memory elements.

14. (original) The array architecture of claim 1, wherein said memory cells comprise polymer memory elements.

15. (original) The array circuit of claim 1, wherein said memory cells comprise phase-changing chalcogenide-based memory elements.

16. canceled

17. (currently amended) A memory device comprising:

at least ~~a~~ two first memory cells;

at least ~~a~~ two second memory cells; and

a gate electrode electrically coupling said first memory cells to said second memory cells, wherein at least one said first memory cell is addressed for reading through at least one said second memory cell and said gate electrode;

wherein said memory cells comprise variable resistance memory elements.

18-21. canceled

22. (currently amended) A memory device comprising: ~~The memory device of claim 17, further comprising:~~

at least a first memory cell;

at least a second memory cell;

a gate electrode electrically coupling said first memory cell to said second memory cell, wherein said first memory cell is addressed for reading through said second memory cell and said gate electrode;

a first bit line in electrical communication with said first memory cell and a sensing circuit;

a second bit line in electrical communication with said second memory cell; and

a wordline in electrical communication with said gate electrode;

wherein said first and second bit lines and said wordline are included in a read circuit which is generated upon grounding of said first bit line, forcing current on said second bit line, and applying voltage to said wordline, said read circuit having a sneak path resistance of $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$, where R is a combined resistance of each said memory cell, n is a number of first memory cells, and m is a total number of wordlines of an array of the memory device.

23. canceled

24. (original) The memory device of claim 17, wherein said first and second memory cells are PCRAM cells.

25. canceled

26. (original) The memory device of claim 17, wherein said first and second memory cells are polymer memory cells.

27. (original) The memory device of claim 17, wherein said first and second memory cells are phase-changing chalcogenide-based memory cells.

28. (currently amended) A processor system, comprising:

a processor; and

a memory circuit, comprising a memory cell block having a plurality of memory cells and a transistor, wherein said memory cells are electrically coupled to

said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor;

wherein said memory cells comprise variable resistance memory elements and at least two memory cells are electrically coupled to each side of said transistor.

29. canceled

30. canceled

31. (previously presented) The processor system of claim 28, wherein each memory cell is in electrical communication with a respective bit line, and at least half of the bit lines are in electrical communication with a sensing circuit.

32. (previously presented) The processor system of claim 28, wherein each memory cell is in electrical communication with a respective bit line, and upon addressing a first memory cell of said memory cell block a sneak path includes any second memory cell of said memory cell block that is electrically coupled to a same side of said transistor as said first memory cell and any third memory cell electrically coupled to a same bit line as said first and second memory cells.

33. canceled

34. (previously presented) The processor system of claim 28, wherein each memory cell is in electrical communication with a respective bit line and said transistor is in electrical communication with a wordline, and a sneak path resistance is $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$, where R is a combined resistance of each said memory cell, n is a number of memory cells of said memory cell block electrically coupled to a same side of said transistor as an addressed memory cell, and m is a total number of wordlines of an array of the memory circuit.

35-39. cancelled

40. (original) The processor system of claim 28, wherein said memory cells comprise PCRAM memory elements.

41. (original) The processor system of claim 28, wherein said memory cells comprise polymer memory elements.

42. (original) The processor system of claim 28, wherein said memory cells comprise phase-changing chalcogenide-based memory elements.

43. canceled

44. (currently amended) A method of reading stored data, comprising:

forming an electrical circuit between an addressed memory cell and a second memory cell, said circuit comprising a transistor gate electrically coupling said addressed memory cell to said second memory cell; ~~and~~

sensing a resistance state of the addressed cell through the circuit; and

calculating a sneak path resistance for said read circuit as [R/(n-1) + [R/(m(n-1))], where R is a combined resistance of each memory cell of said read circuit, n is a number of memory cells electrically coupled to said transistor at a same side as said addressed memory cell, and m is a total number of wordlines,

wherein said memory cells comprise variable resistance memory elements.

45. canceled

46. (original) The method of claim 44, further comprising electrically coupling at least one third memory cell and at least one fourth memory cell to each other through said transistor when said transistor is activated.

47. (original) The method of claim 46, wherein said third memory cell is in electrical communication with a third bit line and said fourth memory cell is in electrical communication with a fourth bit line.

48. canceled

49. (original) The method of claim 44, wherein said addressed memory cell and said second memory cell comprise PCRAM memory elements.

50. (original) The method of claim 44, wherein said addressed memory cell and said second memory cell comprise polymer memory elements.

51. (original) The method of claim 44, wherein said addressed memory cell and said second memory cell comprise phase-changing chalcogenide based memory elements.

52-53. canceled